Remarks:

This amendment is filed with an RCE in response to the final Office Action dated September 1, 2004. Applicant cancels claims 1-16 without prejudice or disclaimer and adds new claims 17-25. Reexamination and early favorable consideration are respectfully requested.

New claims 17-25 are supported by the process illustrated in FIGS. 4-13 and in the accompanying description. Note for example that claim 25 recites the inclusion of a protective film in a wiring structure, which may correspond to the protective film 254 and wiring line 300 shown in FIG. 13.

The final Office Action rejected the prior claims over cited prior art, with U.S. Patent No. 6,319,784 to Yu, et al. (the Yu patent) as the primary reference. U.S. Patent No. 6,596,647 to Kuroda, et al. (the Kuroda patent) is cited as a secondary reference. Applicant submits that the present claims distinguish over the art of record.

The present application is directed to processes for effectively forming semiconductor devices including two or more MISFETs that include at least one P-type MISFET and at least one N-type MISFET. As illustrated in FIG. 2 of the application, planarity and precise formation of contact regions is important to the effective formation of closely spaced P-type and N-type MISFETs.

The application discusses a problem that arises in forming self-aligned silicide ("salicide") contact structures in the presence of oxide shallow trench isolation structures like that illustrated at 20 in FIG. 2. Such structures are significant to forming P-type and N-type MISFETs spaced closely together. "Salicide" processing benefits from very clean silicon surfaces and the application describes using hydrofluoric acid or a similar cleaning solution to provide a clean silicon surface. Use of hydrofluoric acid or a similar cleaning solution can attack

the oxide shallow trench isolation ("STI") structure 20 in FIG. 2, leaving deposits on the surface of the device that can interfere with subsequent processing. These deposits are indicated at 30 in FIG. 3.

The application describes at page 2 a conventional process for cleaning oxide from the surface of doped silicon regions using dilute HF. Because the dilute HF solution breaks down silicon oxide, the cleaning process breaks down silicon oxide from shallow trench isolation structures exposed during the cleaning. SiF_4 is formed as part of the cleaning reaction (see line 17 of page 2) and is deposited on portions of the surface of the doped contact regions. Where the SiF_4 is deposited on the surface of the doped contact regions, the salicide reaction does not occur and poor contacts with high resistance result.

The present application describes the use of a protective film to facilitate the more reliable use of hydrofluoric acid or similar cleaning solutions and to preserve STI structures formed before the cleaning. The process described in the application preserves the quality of salicide contact structures formed in the presence of silicon oxide shallow trench isolation structures used between P-type and N-type MISFETs. These aspects of the disclosed method are emphasized in the present claims, which recite the formation of a protective film in a semiconductor device having at least one P-type MISFET and at least one N-type MISFET.

The Yu patent does not describe devices including at least one P-type MISFET and at least one N-type MISFET and the processing described in the Yu patent is inconsistent with forming devices including at least one P-type MISFET and at least one N-type MISFET. The Kuroda patent does not address this deficiency and similarly does not describe a device including at least one P-type MISFET and at least one N-type MISFET or processes that could be used in forming such a device.

Claim 17 therefore distinguishes over the prior art of record by reciting a "manufacturing method of a semiconductor device including at least two MISFETs, one of which is a P-type MISFET and the other of which is an N-type MISFET" including "covering a surface side of the buried insulating film with a protective film before cleaning the surface side of the semiconductor substrate."

Moreover, the cited Yu patent does not teach forming a protective coating and cleaning a surface using a cleaning solution like dilute HF. The Yu patent seeks to avoid using "an HF dip or sputter etch" in favor of "H_2 annealing." According to column 4, lines 14-16 of the Yu patent, use of the patent's H_2 annealing allows the "HF dip [to] be eliminated resulting in a more environmentally friendly process." Thus, the Yu patent teaches away from claim 17's process of "cleaning a surface side of the semiconductor substrate with a cleaning solution" and refers to the HF dip only in explaining why the process is to be avoided. It would not have been obvious to modify the Yu patent to address this deficiency, because any modification of the Yu patent would follow the Yu patent's teaching the "HF dip" or similar cleaning processes should be avoided.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

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